

Sundaram S S

Hardware Architecture | VLSI & FPGA Engineering | Technical Leadership

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LinkedIn | GitHub | Google Scholar | ResearchGate

Profile

I am a hardware architecture and VLSI engineer with responsibilities in technical leadership, engineering delivery and product planning. Based in Coimbatore, I work across system architecture, Verilog and SystemVerilog RTL, FPGA prototyping, AXI integration and hardware security. I lead design reviews, coordinate teams and milestones, and translate technical priorities into roadmaps and execution plans.

Experience

Deputy Head - Design Process

Zepto Logic Technologies Pvt. Ltd. | Jul 2026 - Present

I lead design-process planning and coordinate technical execution across engineering work. My responsibilities include architecture and design reviews, technology roadmaps, milestone tracking, team guidance, feasibility assessment, and IP/product planning.

Industry contributions: Zero-knowledge proof hardware acceleration; EV inverter hardware-in-the-loop modelling.

Engineering Intern

Aviat Networks | 7 Apr - 31 Dec 2025

On-campus internship on VLAN Switching on Zynq UltraScale+ SoC, with AMD Kria KR260 platform context.

Selected engineering work

Layer-2 Ethernet security firewall

Hardware validated · M.E. thesis

I designed the hardware rule path, packet parser and control structure, integrated the subsystem, and developed the validation flow for my M.E. thesis. The thesis reports a 17-rule hardware implementation using 9.1% of device LUTs and validation with more than 550,000 captured Ethernet frames.

Ethernet processing on Kria KR260

Industry internship · Aviat Networks

I participated in an on-campus engineering internship at Aviat Networks from 7 April to 31 December 2025 on the VLAN-switching project. The experience connected postgraduate VLSI study with an industry engineering environment and FPGA SoC networking.

AXI4 master verification environment

Simulation · SystemVerilog / UVM

I constructed an AXI4 master-side verification environment around sequencer, driver, monitor, scoreboard, and coverage responsibilities. A structured simulation environment with separate stimulus and checking paths for AXI4 master-side protocol behaviour.

Additional engineering studies

FPGA streaming entropy monitor; AXI4-Lite LFSR custom IP; FIR filter PPA characterisation; Schottky diode TCAD study.

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Capabilities, education & research

Technical & professional capabilities

Architecture & integration: System & subsystem architecture; Hardware specifications; AXI4 / AXI4-Lite / AXI-Stream; PS-PL integration; Pipelining & resource sharing.

RTL & FPGA development: Verilog; SystemVerilog; Vivado / Vitis; Zynq-7000; Kria KR260; FPGA prototyping.

Verification & evaluation: Testbench development; UVM environment structure; Protocol checking; Timing & resource analysis; Hardware traffic validation.

Security & research: Hardware network security; Ethernet packet processing; Streaming entropy monitoring; Cryptographic accelerator architecture; Hardware security research.

Engineering leadership & delivery: Design reviews; Team coordination & mentoring; Milestone & action tracking; Cross-functional execution.

Technical strategy & product planning: Technology roadmaps; Feasibility & trade-off analysis; IP maturity assessment; Product positioning & commercialisation planning.

Education

M.E. VLSI Design

PSG College of Technology, Coimbatore | 2024-2026 | CGPA 8.2

B.E. Electrical & Electronics Engineering

Kumaraguru College of Technology, Coimbatore | 2021-2024 | CGPA 8.5

Diploma in Electrical & Electronics Engineering

Kongu Polytechnic College, Perundurai | 2017-2020 | 87%

Publications

Entropy-Driven FPGA-CPU Co-Designed SDN Defence for Resilient Edge Networks. IEEE · ICIET 2025, 2026.

Enhancing Sustainability in Industrial Workspaces: A Smart Approach to CO2 Reduction and Environmental Footprint. Springer · Smart System for Integrated Computing and Communication, 2025.

Sustainable Building Management Through AI, ML, and Advanced Technologies. Springer · Studies in Systems, Decision and Control, Vol. 564, 2024.

An Alternative Approach for Dynamic Wireless Charging. IJARIE · Vol. 9, No. 1, 2023.

Selected training & recognition

Maven Silicon - VLSI SoC Design (Verilog); PSG College of Technology / Qualcomm - System-Level Verification Workshop; IIT Bombay - Spoken Tutorial.

Anna University TN-CEETA Postgraduate Merit Scholar - 88.275 percentile; PSG Achievers Award; Mahatma Gandhi Merit Scholar.

Professional memberships: VLSI Society of India - Tamil Nadu Chapter; International Association of Engineers (IAENG).